General Description

The AAT1112 SwitchReg is a 1.5A step-down converter with an input voltage range of 2.4V to 5.5V and an adjustable output voltage from 0.6V to V_{IN}. The 1.4MHz switching frequency enables the use of small external components. The small footprint and high efficiency make the AAT1112 an ideal choice for portable applications.

The AAT1112 delivers 1.5A maximum output current while consuming only 42µA of no-load quiescent current. Ultra-low $R_{DS(ON)}$ integrated MOSFETs and 100% duty cycle operation make the AAT1112 an ideal choice for high output voltage, high current applications which require a low dropout threshold.

The AAT1112 provides excellent transient response and high output accuracy across the operating range. No external compensation components are required.

The AAT1112 is designed to maintain high efficiency throughout the load range. Pulling the MODE/SYNC pin high enables "PWM Only" mode, maintaining constant frequency and low output ripple across the operating range. Alternatively, the converter may be synchronized to an external clock input via the MODE/SYNC pin. Over-temperature and short-circuit protection safeguard the AAT1112 and system components from damage.

The AAT1112 is available in a Pb-free, space-saving TDFN33-12 or 2.75x3mm TSOPJW-12 package. The product is rated over an operating temperature range of -40°C to +85°C.

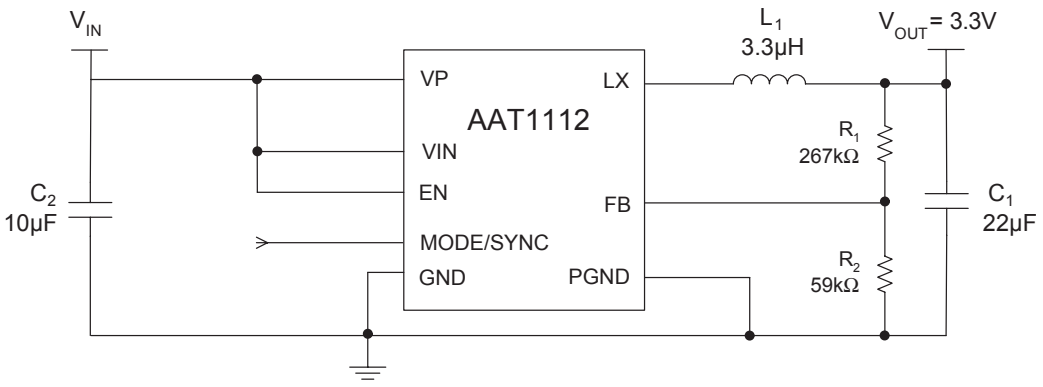
Features

- 1.5A Maximum Output Current
- Input Voltage: 2.4V to 5.5V
- Output Voltage: 0.6V to V_{IN}
- Up to 95% Efficiency
- 42µA No Load Quiescent Current
- No External Compensation Required
- 1.4MHz Switching Frequency
- Synchronizable to External Clock
- Optional "PWM Only" Low Noise Mode
- 100% Duty Cycle Low-Dropout Operation
- Internal Soft Start
- Over-Temperature and Current Limit Protection
- <1µA Shutdown Current
- TSOPJW-12 or TDFN33-12 Package
- Temperature Range: -40°C to +85°C

Applications

- Cellular Phones
- Digital Cameras
- Hard Disk Drives
- MP3 Players
- PDAs and Handheld Computers
- Portable Media Players
- USB Devices

Typical Application

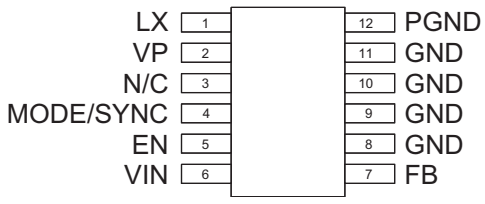


Pin Descriptions

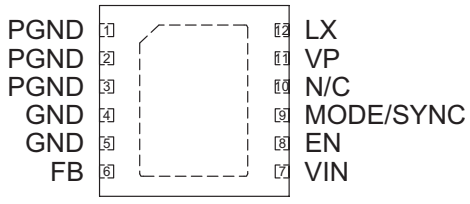
Pin # TSOPJW-12	Pin # TDFN33-12	Symbol	Function
1	12	LX	Switching node. Connect the output inductor to this pin. The switching node is internally connected to the drain of both high- and low-side MOSFETs.
2	11	VP	Input voltage for the power switches.
3	10	N/C	Not connected.
4	9	MODE/SYNC	Connect to ground for PFM/PWM mode and optimized efficiency throughout the load range. Connect high for low noise PWM operation under all operating conditions. Connect to an external clock for synchronization (PWM only).
5	8	EN	Enable pin. A logic low disables the converter and it consumes less than 1µA of current. When connected high, it resumes normal operation.
6	7	VIN	Power supply. Supplies power for the internal circuitry.
7	6	FB	Feedback input pin. This pin is connected either directly to the converter output or to an external resistive divider for an adjustable output.
8, 9, 10, 11	4, 5	GND	Non-power signal ground pin.
12	1, 2, 3	PGND	Main power ground return pin. Connect to the output and input capacitor return.
N/A	EP		Exposed paddle (bottom); connect to ground as closely as possible to the device.

Pin Configuration

TSOPJW-12
(Top View)



TDFN33-12
(Top View)



Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
V_{IN}	VIN, VP to GND	6.0	V
V_{LX}	LX Pin to GND	-0.3 to V_{IN} + 0.3	V
V_{FB}	FB Pin to GND	-0.3 to V_{IN} + 0.3	V
V_N	MODE/SYNC, EN to GND	-0.3 to 6.0	V
T_J	Operating Junction Temperature Range	-40 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	300	°C

Thermal Information

Symbol	Description		Value	Units
P_D	Maximum Power Dissipation	TSOPJW-12	0.625	W
		TDFN33-12	2.0	
θ_{JA}	Thermal Resistance[2]	TSOPJW-12	160	°C/W
		TDFN33-12	50	

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Mounted on an FR4 board.

Electrical Characteristics[1]

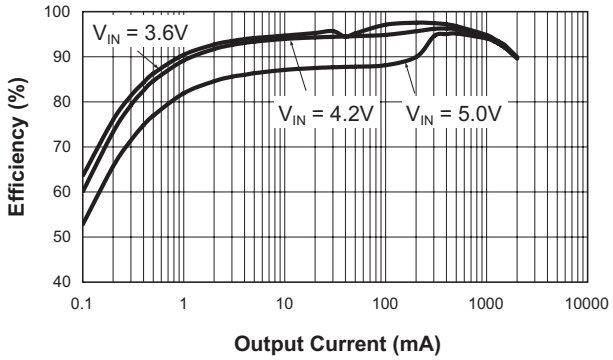
V_{IN} = 3.6V; T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage		2.4		5.5	V
V_{OUT}	Output Voltage Range		0.6		V_{IN}	V
V_{UVLO}	UVLO Threshold	V_{IN} Rising			2.4	V
		Hysteresis		250		mV
		V_{IN} Falling	1.8			V
V_{OUT}	Output Voltage Tolerance	I_{OUT} = 0A to 1.5A, V_{IN} = 2.4V to 5.5V	-3.0		3.0	%
I_Q	Quiescent Current	No Load		42	90	µA
I_{SHDN}	Shutdown Current	V_{EN} = GND			1.0	µA
I_{LIM}	Current Limit		1.8			A
$R_{DS(ON)H}$	High Side Switch On-Resistance			0.120		Ω
$R_{DS(ON)L}$	Low Side Switch On-Resistance			0.085		Ω
I_{LXLEAK}	LX Leakage Current	V_{IN} = 5.5V, V_{LX} = 0 to V_{IN}			1.0	µA
$I_{LXLK, R}$	LX Reverse Leakage Current	V_{IN} Unconnected, V_{LX} = 5.5V, V_{EN} = GND			1.0	µA
$\Delta V_{LOADREG}$	Load Regulation	I_{LOAD} = 0A to 1.5A		0.5		%
$\Delta V_{LINEREG}/\Delta V_{IN}$	Line Regulation	V_{IN} = 2.4V to 5.5V		0.2		%/V
V_{FB}	Feedback Threshold Voltage Accuracy (Adjustable Version)	No Load, T_A = 25°C	0.591	0.60	0.609	V
I_{FB}	FB Leakage Current	V_{OUT} = 1.0V			0.2	µA
F_{OSC}	Internal Oscillator Frequency		1.12	1.4	1.68	MHz
	Synchronous Clock		0.60		3.0	
T_S	Start-Up Time	From Enable to Output Regulation		150		µs
T_{SD}	Over-Temperature Shutdown Threshold			140		°C
T_{HYS}	Over-Temperature Shutdown Hysteresis			15		°C
EN						
V_{IL}	Enable Threshold Low				0.6	V
V_{IH}	Enable Threshold High		1.4			V
I_{EN}	Enable Leakage Current	V_{IN} = V_{EN} = 5.5V	-1.0		1.0	µA
MODE/SYNC						
$V_{MODE/SYNC(L)}$	Enable Threshold Low				0.6	V
$V_{MODE/SYNC(H)}$	Enable Threshold High		1.4			V
$I_{MODE/SYNC}$	Enable Leakage Current	V_{IN} = V_{EN} = 5.5V	-1.0		1.0	µA

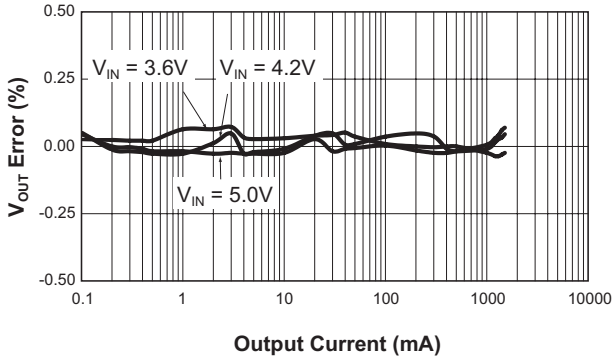
1. The AAT1112 is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range and is assured by design, characterization, and correlation with statistical process controls.

Typical Characteristics

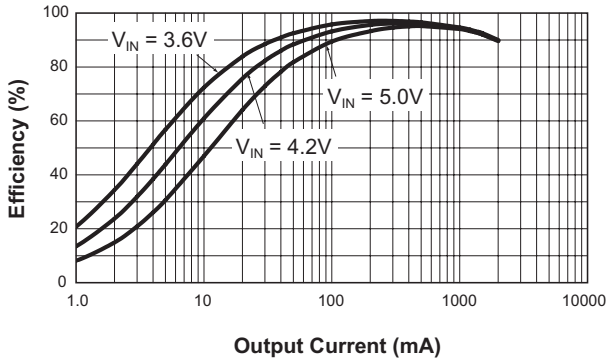
Efficiency vs. Output Current
(PFM Mode; V_{OUT} = 3.3V)



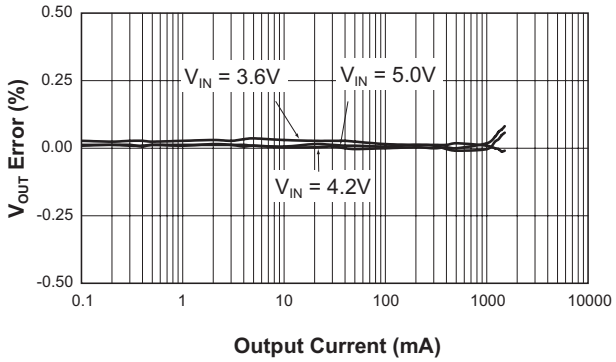
Load Regulation
(PFM Mode; V_{OUT} = 3.3V)



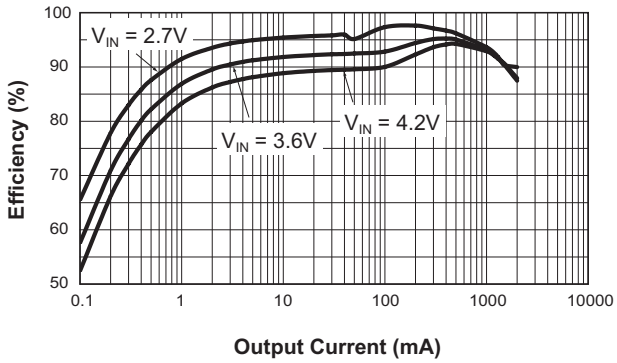
Efficiency vs. Output Current
(PWM Mode; V_{OUT} = 3.3V)



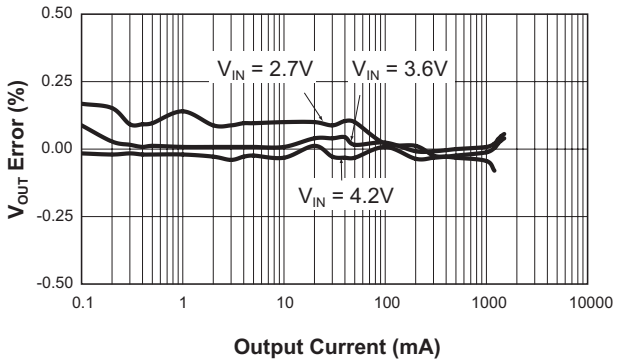
Load Regulation
(PWM Mode; V_{OUT} = 3.3V)



Efficiency vs. Output Current
(PFM Mode; V_{OUT} = 2.5V)

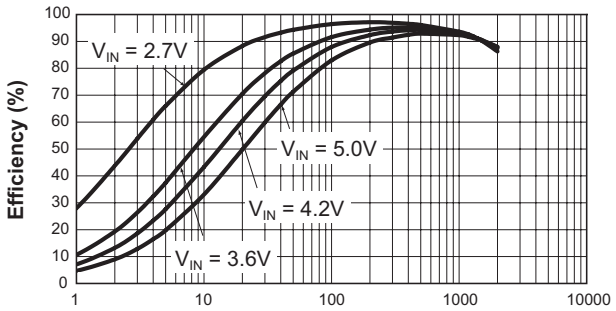


Load Regulation
(PFM Mode; V_{OUT} = 2.5V)

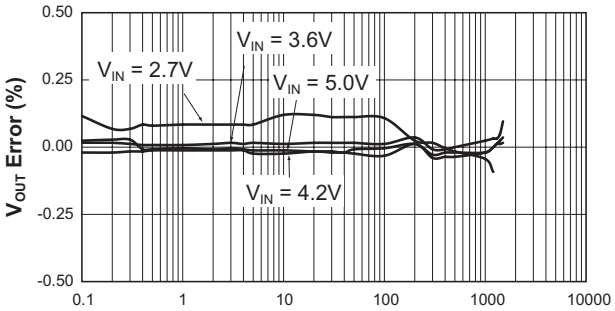


Typical Characteristics

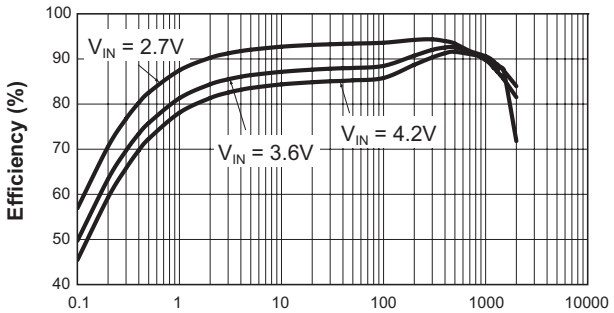
Efficiency vs. Output Current
(PWM Mode; V_{OUT} = 2.5V)



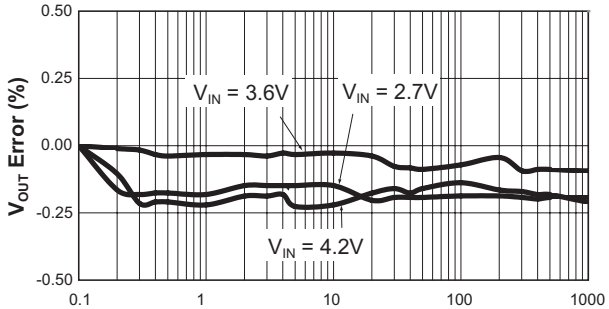
Load Regulation
(PWM Mode; V_{OUT} = 2.5V)



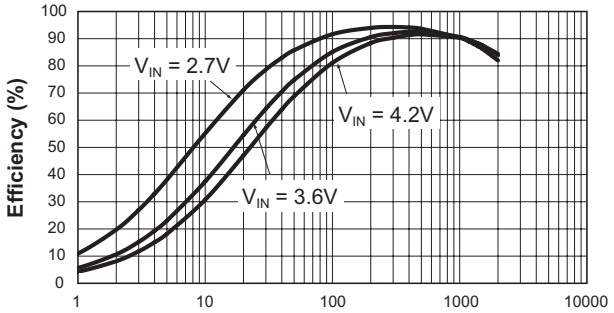
Efficiency vs. Output Current
(PFM Mode; V_{OUT} = 1.8V)



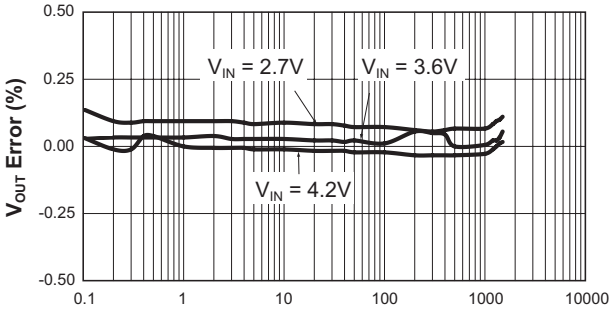
Load Regulation
(PFM Mode; V_{OUT} = 1.8V)



Efficiency vs. Output Current
(PWM Mode; V_{OUT} = 1.8V)

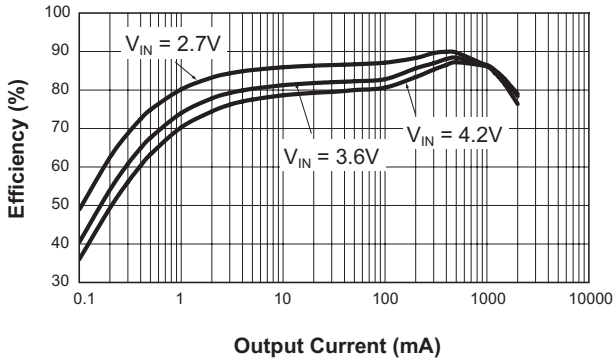


Load Regulation
(PWM Mode; V_{OUT} = 1.8V)

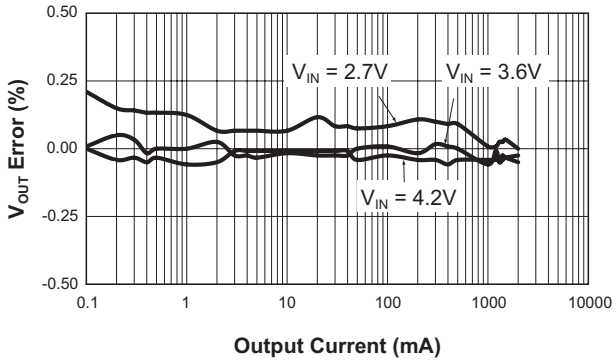


Typical Characteristics

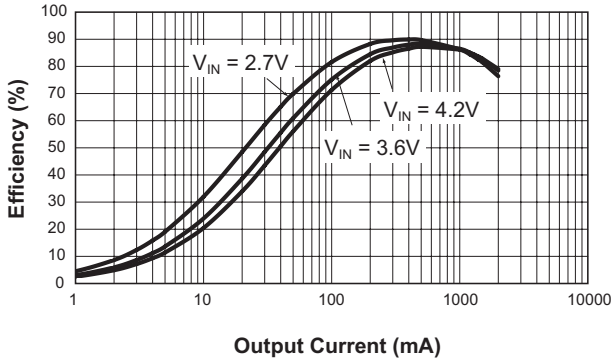
Efficiency vs. Output Current
(PFM Mode; V_{OUT} = 1.2V)



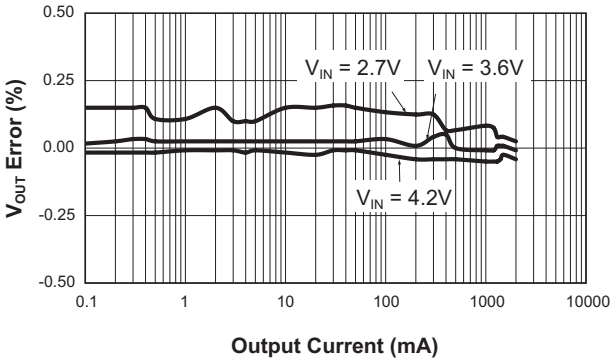
Load Regulation
(PFM Mode; V_{OUT} = 1.2V)



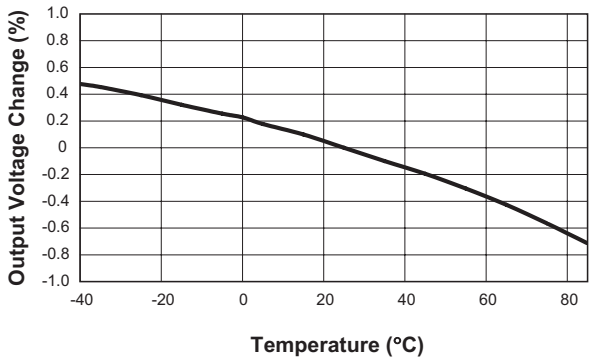
Efficiency vs. Output Current
(PWM Mode; V_{OUT} = 1.2V)



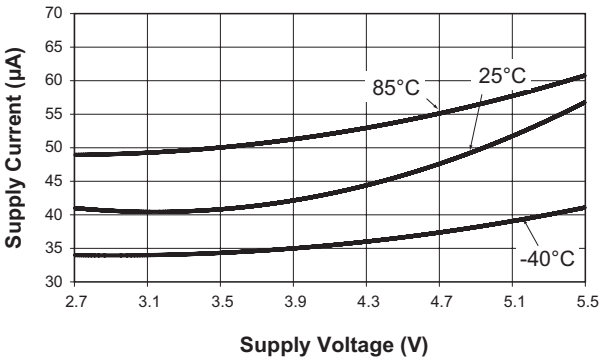
Load Regulation
(PWM Mode; V_{OUT} = 1.2V)



Output Voltage vs. Temperature
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 1A)

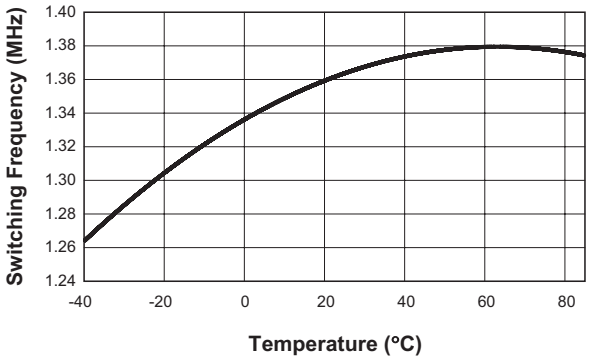


Supply Current vs. Supply Voltage
(V_{OUT} = 1.8V; No Load; PFM Mode)

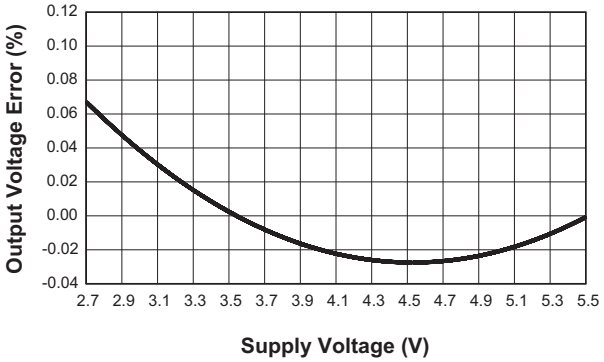


Typical Characteristics

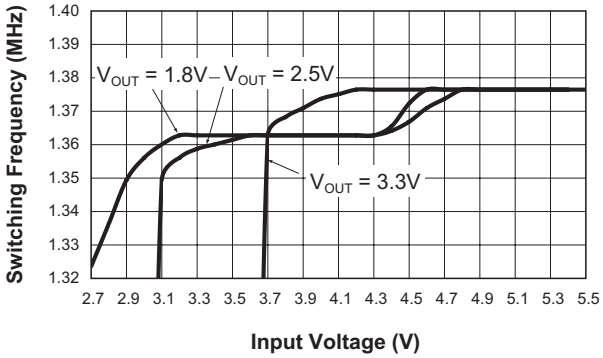
Switching Frequency vs. Temperature
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 1A)



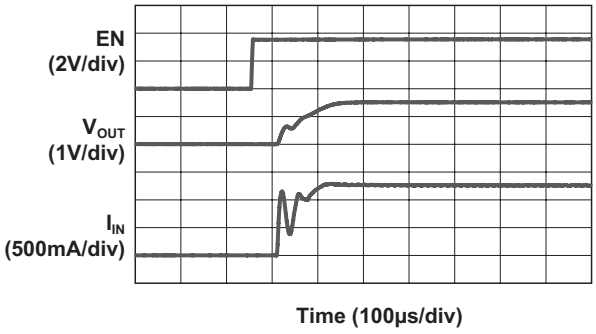
Line Regulation
(V_{OUT} = 1.8V; I_{OUT} = 1A)



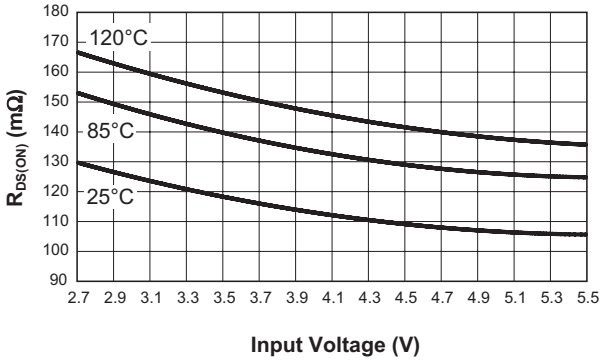
Switching Frequency vs. Input Voltage
(I_{OUT} = 1A)



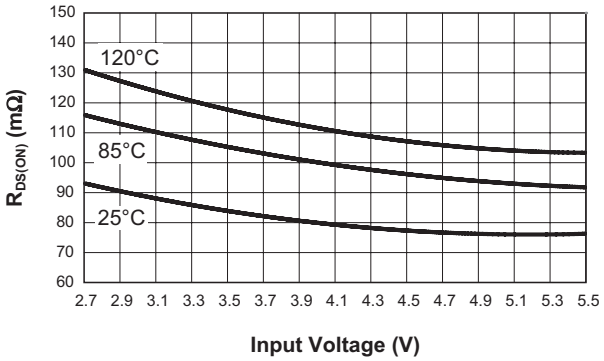
Enable Soft Start
(V_{OUT} = 3.6V; I_{OUT} = 1.5A)



P-Channel $R_{DS(ON)}$ vs. Input Voltage

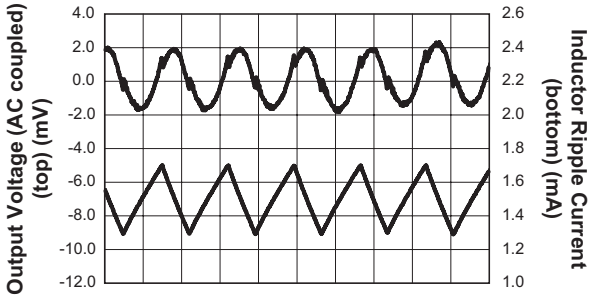


N-Channel $R_{DS(ON)}$ vs. Input Voltage



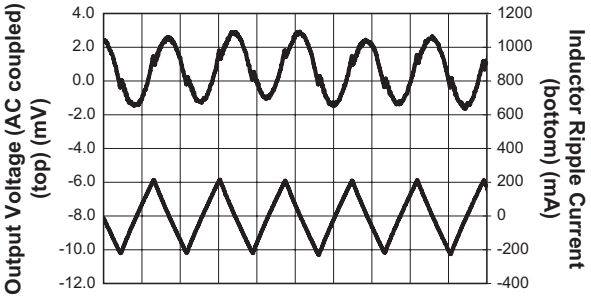
Typical Characteristics

Heavy Load Switching Waveform
(V_{IN} = 3.6V; V_{OUT} = 1.8V; 1.5A Load)



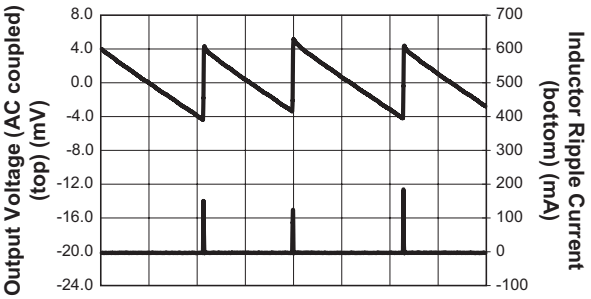
Time (2.5µs/div)

Light Load Switching Waveform
(V_{IN} = 3.6V; V_{OUT} = 1.8V; 1mA Load)



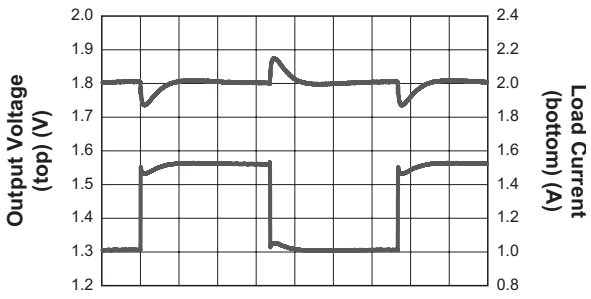
Time (2.5µs/div)

Light Load Switching Waveform
(V_{IN} = 3.6V; V_{OUT} = 1.8V; 1mA Load)



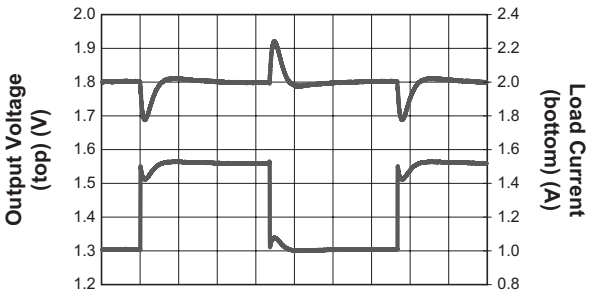
Time (100µs/div)

Load Transient Response
(V_{IN} = 3.6V; V_{OUT} = 1.8V; C_{FF} = 100pF)



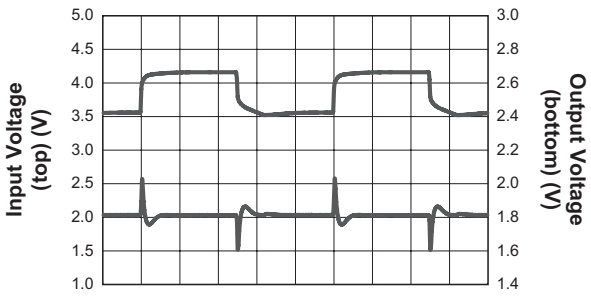
Time (20µs/div)

Load Transient Response
(V_{IN} = 3.6V; V_{OUT} = 1.8V; No C_{FF})



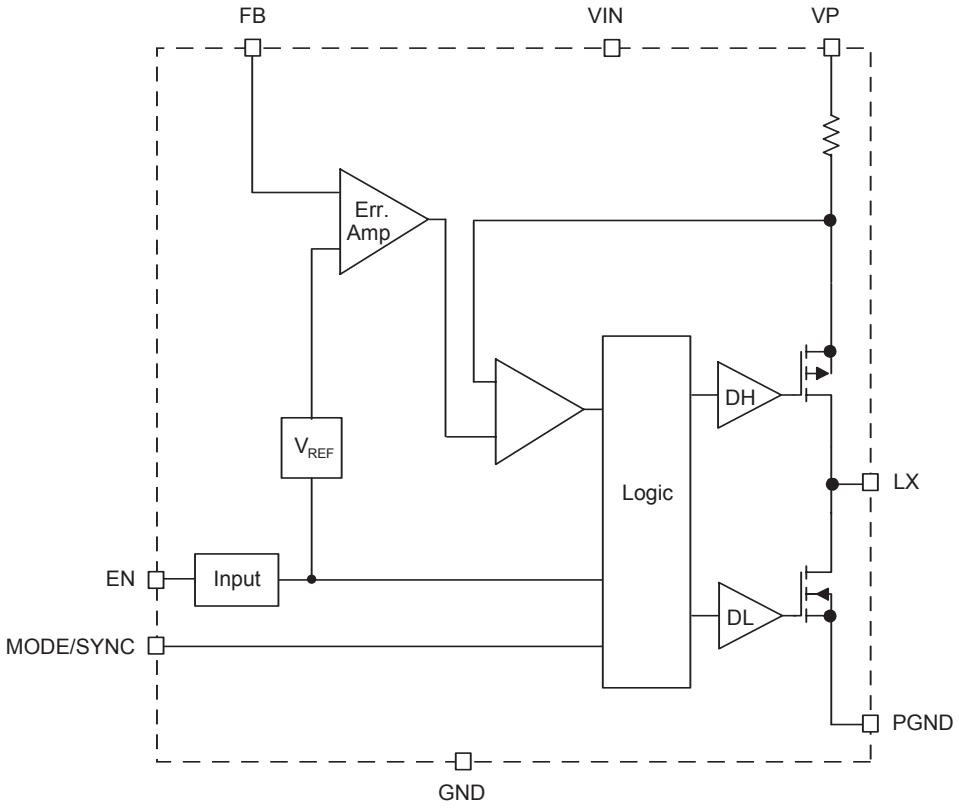
Time (20µs/div)

Line Transient Response
(V_{OUT} = 1.8V; 1.5A Load)



Time (200µs/div)

Functional Block Diagram



Functional Description

The AAT1112 is a high performance 1.5A monolithic step-down converter operating at 1.4MHz switching frequency. It minimizes external component size and optimizes efficiency over the complete load range. Apart from the small bypass input capacitor, only a small L-C filter is required at the output. Typically, a 3.3µH inductor and a 22µF ceramic capacitor are recommended for a 3.3V output (see table of recommended values).

At dropout, the converter duty cycle increases to 100% and the output voltage tracks the input voltage minus the $R_{DS(ON)}$ drop of the P-channel high-side MOSFET (plus the DC drop of the external inductor). The device integrates extremely low $R_{DS(ON)}$ MOSFETs to achieve low dropout voltage during 100% duty cycle operation. This is advantageous in applications requiring high output voltages (typically > 2.5V) at low input voltages.

The integrated low-loss MOSFET switches can provide greater than 95% efficiency at full load. PFM operation maintains high efficiency under light load conditions (typically <150mA). The MODE/SYNC pin allows optional "PWM only" mode. This maintains constant frequency and low output ripple across all load conditions. Alternatively, the IC can be synchronized to an external clock via the MODE/ SYNC input. External synchronization is maintained between 0.6MHz and 3.0MHz.

In battery-powered applications, as V_{IN} decreases, the converter dynamically adjusts the operating frequency prior to dropout to maintain the required duty cycle and provide accurate output regulation.

Output regulation is maintained until the dropout voltage, or minimum input voltage, is reached. At 1.5A output load, dropout voltage headroom is approximately 200mV.

The AAT1112 typically achieves better than ±0.5% output regulation across the input voltage and output load range. A current limit of 2.0A (typical) protects the IC and system components from short-circuit damage. Typical no load quiescent current is 42µA.

Thermal protection completely disables switching when the maximum junction temperature is detected. The junction over-temperature threshold is 140°C with 15°C of hysteresis. Once an over-temperature or over-current fault condition is removed, the output voltage automatically recovers.

Peak current mode control and optimized internal compensation provide high loop bandwidth and excellent response to input voltage and fast load transient events. Soft start eliminates output voltage overshoot when the enable or the input voltage is applied. Under-voltage lockout prevents spurious start-up events.

Control Loop

The AAT1112 is a peak current mode step-down converter. The current through the P-channel MOSFET (high side) is sensed for current loop control, as well as short-circuit and overload protection. A fixed slope compensation signal is added to the sensed current to maintain stability for duty cycles greater than 50%. The peak current mode loop appears as a voltage-programmed current source in parallel with the output capacitor.

The output of the voltage error amplifier programs the current mode loop for the necessary peak switch current to force a constant output voltage for all load and line conditions. Internal loop compensation terminates the transconductance voltage error amplifier output. The reference voltage is internally set to program the converter output voltage greater than or equal to 0.6V.

Soft Start/Enable

Soft start limits the current surge seen at the input and eliminates output voltage overshoot. When pulled low, the enable input forces the AAT1112 into a low-power, non-switching state. The total input current during shutdown is less than 1µA.

Current Limit and Over-Temperature Protection

For overload conditions, the peak input current is limited. To minimize power dissipation and stresses under current limit and short-circuit conditions, switching is terminated after entering current limit for a series of pulses. Switching is terminated for seven consecutive clock cycles after a current limit has been sensed for a series of four consecutive clock cycles.

Thermal protection completely disables switching when internal dissipation becomes excessive. The junction over-temperature threshold is 140°C with 15°C of hysteresis. Once an over-temperature or over-current fault conditions is removed, the output voltage automatically recovers.

Under-Voltage Lockout

Internal bias of all circuits is controlled via the VIN input. Under-voltage lockout (UVLO) guarantees sufficient V_{IN} bias and proper operation of all internal circuitry prior to activation.

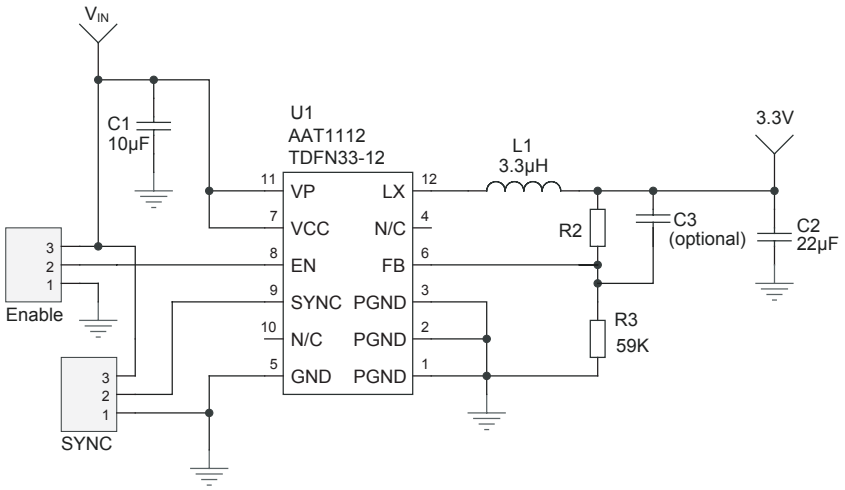


Figure 1: AAT1112 Schematic.

Component Selection

Inductor Selection

The step-down converter uses peak current mode control with slope compensation to maintain stability for duty cycles greater than 50%. The output inductor value must be selected so the inductor current down slope meets the internal slope compensation requirements. The inductor should be set equal to the output voltage numeric value in µH. This guarantees that there is sufficient internal slope compensation.

Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR. Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor.

The 3.3µH CDRH4D28 series Sumida inductor has a 49.2mΩ worst case DCR and a 1.57A DC current rating. At full 1.5A load, the inductor DC loss is 97mW which gives less than 1.5% loss in efficiency for a 1.5A, 3.3V output.

Input Capacitor

Select a 10µF to 22µF X7R or X5R ceramic capacitor for the input. To estimate the required input capacitor size, determine the acceptable input ripple level (V_{PP}) and solve for C. The calculated value varies with input voltage and is a maximum when V_{IN} is double the output voltage.

$$C_{IN} = \frac{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot F_S}$$

$$\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right) = \frac{1}{4} \text{ for } V_{IN} = 2 \cdot V_O$$

$$C_{IN(MIN)} = \frac{1}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot 4 \cdot F_S}$$

Always examine the ceramic capacitor DC voltage coefficient characteristics when selecting the proper value. For example, the capacitance of a 10µF, 6.3V, X5R ceramic capacitor with 5.0V DC applied is actually about 6µF.

The maximum input capacitor RMS current is:

$$I_{RMS} = I_O \cdot \sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}$$

The input capacitor RMS ripple current varies with the input and output voltage and will always be less than or equal to half of the total DC load current.

$$\sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)} = \sqrt{D \cdot (1 - D)} = \sqrt{0.5^2} = \frac{1}{2}$$

for $V_{IN} = 2 \cdot V_O$

$$I_{RMS(MAX)} = \frac{I_O}{2}$$

The term $\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)$ appears in both the input voltage ripple and input capacitor RMS current equations and is a maximum when V_O is twice V_{IN}. This is why the input voltage ripple and the input capacitor RMS current ripple are a maximum at 50% duty cycle.

The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the AAT1112. Low ESR/ESL X7R and X5R ceramic capacitors are ideal for this function. To minimize stray inductance, the capacitor should be placed as closely as possible to the IC. This keeps the high frequency content of the input current localized, minimizing EMI and input voltage ripple.

The proper placement of the input capacitor (C1) can be seen in the evaluation board layout in the Layout section of this datasheet (see Figure 2).

A laboratory test set-up typically consists of two long wires running from the bench power supply to the evaluation board input voltage pins. The inductance of these wires, along with the low-ESR ceramic input capacitor, can create a high Q network that may affect converter performance. This problem often becomes apparent in the form of excessive ringing in the output voltage during load transients. Errors in the loop phase and gain measurements can also result.

Since the inductance of a short PCB trace feeding the input voltage is significantly lower than the power leads from the bench power supply, most applications do not exhibit this problem.

In applications where the input power source lead inductance cannot be reduced to a level that does not affect the converter performance, a high ESR tantalum or aluminum electrolytic should be placed in parallel with the low ESR/ESL bypass ceramic capacitor. This dampens the high Q network and stabilizes the system.

Output Capacitor

The output capacitor limits the output ripple and provides holdup during large load transitions. A 10µF to 22µF X5R or X7R ceramic capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions and has the ESR and ESL characteristics necessary for low output ripple.

The output voltage droop due to a load transient is dominated by the capacitance of the ceramic output capacitor. During a step increase in load current, the ceramic output capacitor alone supplies the load current until the loop responds. Within two or three switching cycles, the loop responds and the inductor current increases to match the load current demand. The relationship of the output voltage droop during the three switching cycles to the output capacitance can be estimated by:

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S}$$

Once the average inductor current increases to the DC load level, the output voltage recovers. The above equation establishes a limit on the minimum value for the output capacitor with respect to load transients.

The internal voltage loop compensation also limits the minimum output capacitor value to 10µF. This is due to its effect on the loop crossover frequency (bandwidth), phase margin, and gain margin. Increased output capacitance will reduce the crossover frequency with greater phase margin.

Adjustable Output Resistor Selection

The output voltage on the AAT1112 is programmed with external resistors R1 and R2. To limit the bias current required for the external feedback resistor string while maintaining good noise immunity, the minimum suggested value for R2 is 59kΩ. Although a larger value will further reduce quiescent current, it will also increase the impedance of the feedback node, making it more sensitive to external noise and interference. Table 1 summarizes the resistor values for various output voltages with R2 set to either 59kΩ for good noise immunity or 221kΩ for reduced no load input current.

	R2 = 59kΩ	R2 = 221kΩ
V_{OUT} (V)	R1 (kΩ)	R1 (kΩ)
0.8	19.6	75
0.9	29.4	113
1.0	39.2	150
1.1	49.9	187
1.2	59.0	221
1.3	68.1	261
1.4	78.7	301
1.5	88.7	332
1.8	118	442
1.85	124	464
2.0	137	523
2.5	187	715
3.0	237	887
3.3	267	1000

Table 1: AAT1112 Resistor Values for Various Output Voltages.

Thermal Calculations

There are three types of losses associated with the AAT1112 step-down converter: switching losses, conduction losses, and quiescent current losses. Conduction losses are associated with the $R_{DS(ON)}$ characteristics of the power output switching devices. Switching losses are dominated by the gate charge of the power output switching devices. At full load, assuming continuous conduction mode (CCM), a simplified form of the losses is given by:

$$P_{TOTAL} = \frac{I_O^2 \cdot (R_{DS(ON)H} \cdot V_O + R_{DS(ON)L} \cdot [V_{IN} - V_O])}{V_{IN}}$$

$$+ (t_{sw} \cdot F_S \cdot I_O + I_Q) \cdot V_{IN}$$

I_Q is the step-down converter quiescent current. The term t_{sw} is used to estimate the full load step-down converter switching losses.

For the condition where the step-down converter is in dropout at 100% duty cycle, the total device dissipation reduces to:

$$P_{TOTAL} = I_O^2 \cdot R_{DS(ON)H} + I_Q \cdot V_{IN}$$

Since $R_{DS(ON)}$, quiescent current, and switching losses all vary with input voltage, the total losses should be investigated over the complete input voltage range.

Given the total losses, the maximum junction temperature can be derived from the θ_{JA} for the TDFN3-12 and TSOPJW-12 packages, which is 50°C/W and 160°C/W respectively.

$$T_{J(MAX)} = P_{TOTAL} \cdot \Theta_{JA} + T_{AMB}$$

Layout

The suggested PCB layout for the AAT1112 is shown in Figures 2 and 3. The following guidelines should be used to help ensure a proper layout.

1. The input capacitor (C1) should connect as closely as possible to VP and PGND.
2. C2 and L1 should be connected as closely as possible. The connection of L1 to the LX pin should be as short as possible.
3. The feedback trace or FB pin should be separate from any power trace and connect as closely as possible to the load point. Sensing along a high-current load trace will degrade DC load regulation.
4. The resistance of the trace from the load return to PGND should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.
5. Connect unused signal pins to ground to avoid unwanted noise coupling.

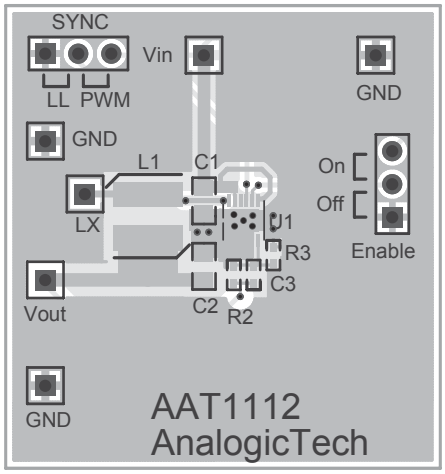


Figure 2: AAT1112 Evaluation Board Top Side Layout.

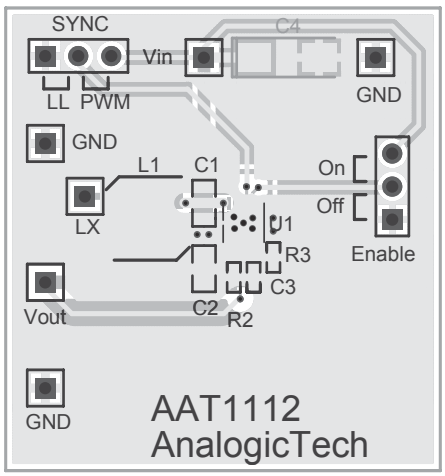


Figure 3: AAT1112 Evaluation Board Bottom Side Layout.

Design Example

Specifications

V_O 3.3V @ 1.5A, Pulsed Load ΔI_{LOAD} = 1.5A

V_{IN} 2.7V to 4.2V (3.6V nominal)

F_S 1.2MHz

T_{AMB} 85°C in TDFN33-12 Package

Output Inductor

L1 = V_O(µH) = 3.3µH; see Table 2.

For Sumida inductor CDRH4D28 3.3µH DCR = 49.2mΩ max.

$$\Delta I_1 = \frac{V_O}{L1 \cdot F_S} \cdot \left(1 - \frac{V_{O1}}{V_{IN}}\right) = \frac{3.3V}{3.3\mu H \cdot 1.2MHz} \cdot \left(1 - \frac{3.3V}{4.2V}\right) = 179mA$$

$$I_{PK1} = I_{O1} + \frac{\Delta I_1}{2} = 1.5A + 0.089A = 1.59A$$

$$P_{L1} = I_{O1}^2 \cdot DCR = 1.5A^2 \cdot 49.2m\Omega = 110mW$$

Output Capacitor

V_{DROOP} = 0.2V

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S} = \frac{3 \cdot 1.5A}{0.2V \cdot 1.2MHz} = 18.8\mu F; \text{ use } 22\mu F$$

$$I_{RMS(MAX)} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{(V_{OUT}) \cdot (V_{IN(MAX)} - V_{OUT})}{L \cdot F_S \cdot V_{IN(MAX)}} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{3.3V \cdot (4.2V - 3.3V)}{3.3\mu H \cdot 1.2MHz \cdot 4.2V} = 52mArms$$

$$P_{esr} = esr \cdot I_{RMS}^2 = 5m\Omega \cdot (52mA)^2 = 13.3\mu W$$

Input Capacitor

Input Ripple V_{PP} = 50mV

$$C_{IN} = \frac{1}{\left(\frac{V_{PP}}{I_{O1} + I_{O2}} - ESR\right) \cdot 4 \cdot F_S} = \frac{1}{\left(\frac{50mV}{1.5A} - 5m\Omega\right) \cdot 4 \cdot 1.2MHz} = 7.3\mu F; \text{ use } 10\mu F$$

$$I_{RMS(MAX)} = \frac{I_O}{2} = 0.75Arms$$

$$P = esr \cdot I_{RMS}^2 = 5m\Omega \cdot (0.75A)^2 = 3mW$$

AAT1112 Losses

Total losses can be estimated by calculating the dropout ($V_{IN} = V_O$) losses where the power MOSFET $R_{DS(ON)}$ will be at the maximum value. All values assume an 85°C ambient temperature and a 120°C junction temperature with the TDFN 50°C/W package.

$$P_{LOSS} = I_{O1}^2 \cdot R_{DS(ON)H} = 1.5A^2 \cdot 0.16\Omega = 0.36W$$

$$T_{J(MAX)} = T_{AMB} + \Theta_{JA} \cdot P_{LOSS} = 85°C + (50°C/W) \cdot 360mW = 103°C$$

The total losses are also investigated at the nominal lithium-ion battery voltage (3.6V). The simplified version of the $R_{DS(ON)}$ losses assumes that the N-channel and P-channel $R_{DS(ON)}$ are equal.

$$P_{TOTAL} = I_O^2 \cdot R_{DS(ON)} + (t_{sw} \cdot F_S \cdot I_O + I_Q) \cdot V_{IN}$$

$$= 1.5A^2 \cdot 152m\Omega + (5ns \cdot 1.2MHz \cdot 1.5A + 50\mu A) \cdot 3.6V = 375mW$$

$$T_{J(MAX)} = T_{AMB} + \Theta_{JA} \cdot P_{LOSS} = 85°C + (50°C/W) \cdot 375mW = 104°C$$

V_{OUT} (V)	Inductance (µH)	Part Number	Manufacturer	Size (mm)	Rated Current (A)	I_{RMS} (A)	I_{SAT} (A)	DCR (Ω)
3.3	3.3	CDRH4D28	Sumida	5x5x3	1.57			36.4
2.5	2.2	CDRH4D28	Sumida	5x5x3	2.04			23.2
1.8	1.8	CDRH4D28	Sumida	5x5x3	2.2			20.4
1.5	1.8	CDRH4D28	Sumida	5x5x3	2.2			20.4
1.2	1.2	CDRH4D28	Sumida	5x5x3	2.56			17.5
1.0	1.0	SD3114-1.0	Cooper	3.1x3.1x1.45		1.67	2.07	0.042
0.8	1.0	SD3114-1.0	Cooper	3.1x3.1x1.45		1.67	2.07	0.042
0.6	1.0	SD3114-1.0	Cooper	3.1x3.1x1.45		1.67	2.07	0.042

Table 2: Surface Mount Inductors.

Manufacturer	Part Number	Value	Voltage	Temp. Co.	Case
MuRata	GRM21BR60J106KE19	10µF	6.3V	X5R	0805
MuRata	GRM21BR60J226ME39	22µF	6.3V	X5R	0805

Table 3: Surface Mount Capacitors.

Ordering Information

Package	Marking[1]	Part Number (Tape and Reel)[2]
TSOPJW-12		AAT1112ITP-0.6-T1
TDFN33-12	SBXYY	**AAT1112IWP-0.6-T1**

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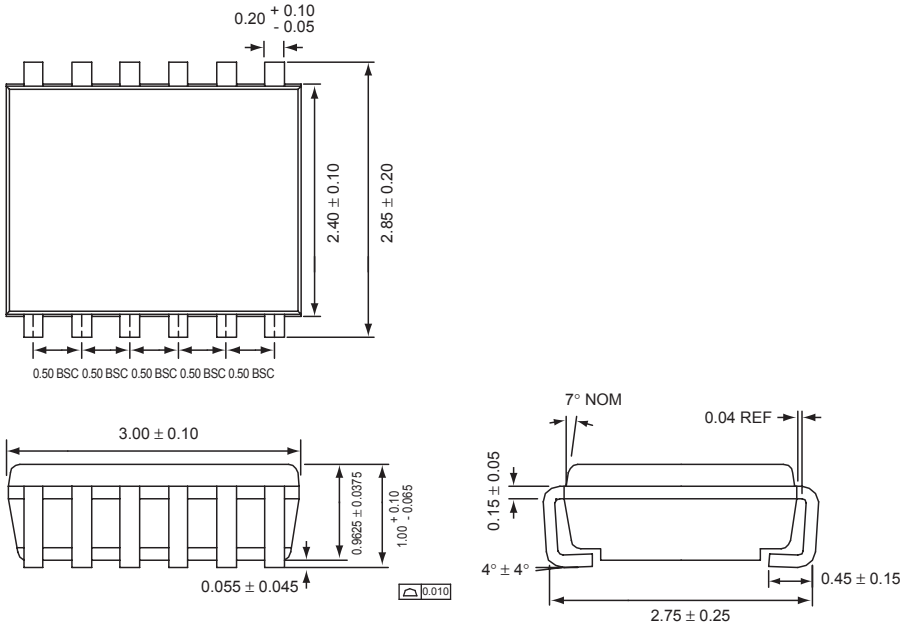
Package Information[3]

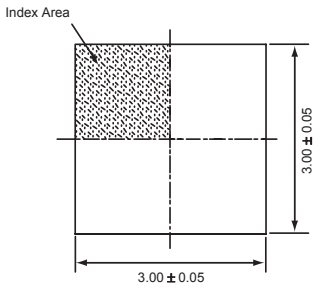
TSOPJW-12



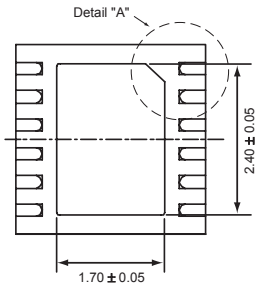
All dimensions in millimeters.

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.
3. The leadless package family, which includes QFN, TQFN, DFN, TDFN and STDFN, has exposed copper (unplated) at the end of the lead terminals due to the manufacturing process. A solder fillet at the exposed copper edge cannot be guaranteed and is not required to ensure a proper bottom solder connection.

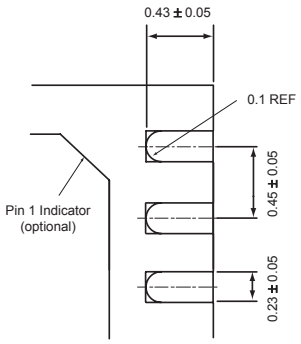
TDFN33-12



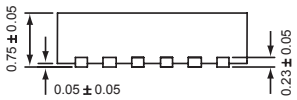
Top View



Bottom View



Detail "A"



Side View

All dimensions in millimeters.

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